Icemos
Cooler than cool

Preliminary Data Sheet

ICE30N60W

ICE30N60W N-Channel Enhancement Mode MOSFET

RoHS compliant 2011/65/EU

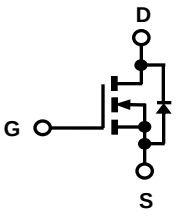
CE

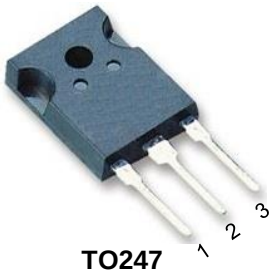
HALOGEN FREE

Product Summary			
I_D	T_A=25°C	30A	Max
$V_{(BR)DSS}$	I_D=250uA	600V	Min
$r_{DS(on)}$	V_{GS}=10V	0.075Ω	Typ
Q_g	V_{DS}=480V	187nC	Typ

Features

- TO247 package
- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





TO247
1:G, 2:D,
3:S, 4:D,

(TO-247)

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [b] , at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C	30	A
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	103	A
Avalanche energy, single pulse	E_{AS}	I_D=18A	1100	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	18	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=30A, T_j=125°C	50	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	313	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C
Mounting torque		M 3 & 3.5 screws	60	Ncm

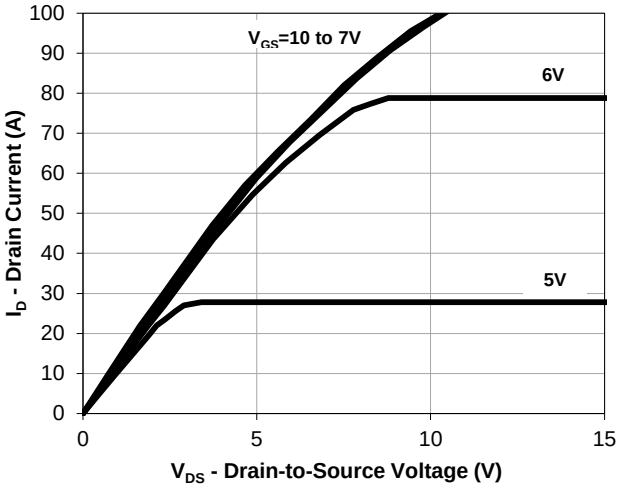
a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

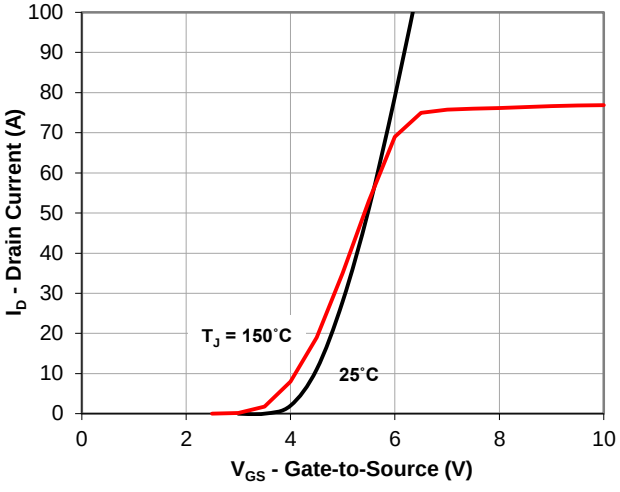
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Thermal characteristics						
Thermal resistance, junction-case [a]	R_{thJC}		-	-	0.3	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	50	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C
Electrical characteristics [b], at T_j=25°C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1mA	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C	-	0.5	10	μA
		V_{DS}=600V, V_{GS}=0V, T_j=150°C	-	-	250	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	200	nA
Drain-source on-state resistance	$R_{DS\ (on)}$	V_{GS}=10V, I_D=15A, T_j=25°C	-	0.075	0.09	Ω
		V_{GS}=10V, I_D=15A, T_j=150°C	-	0.2	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	6	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	5970	-	pF
Output capacitance	C_{oss}		-	677	-	
Reverse transfer capacitance	C_{rss}		-	35	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=15A	-	30	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=380V, V_{GS}=10V, I_D=30A, R_G=4Ω (External)	-	160	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	25	-	

Parameter	*Symbol*	*Conditions*	*Values*			*Unit*
			Min	*Typ*	*Max*	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=30A, V_{GS}=0 to 10 V	-	36	-	nC
Gate to drain charge	Q_{gd}		-	62	-	
Gate charge total	Q_g		-	187	-	
Gate plateau voltage	$V_{plateau}$		-	5.3	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0V, I_S=I_F	-	0.95	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=480V, I_S=I_F, d_{iF}/d_t=100 A/µS	-	547	-	ns
Reverse recovery charge	Q_{rr}		-	12	-	µC
Peak reverse recovery current	I_{rm}		-	43	-	A

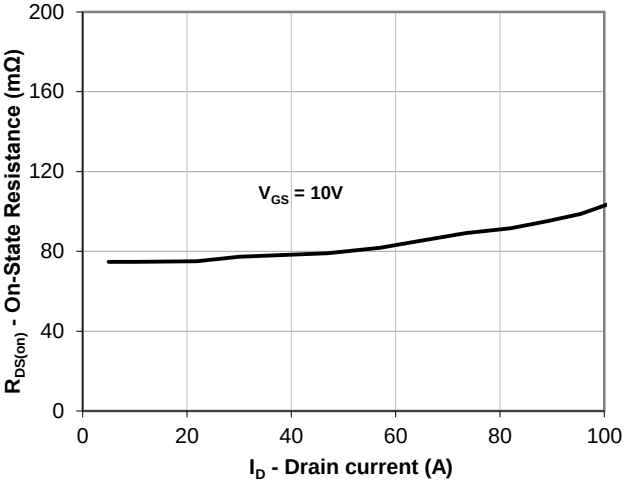
Output Characteristics



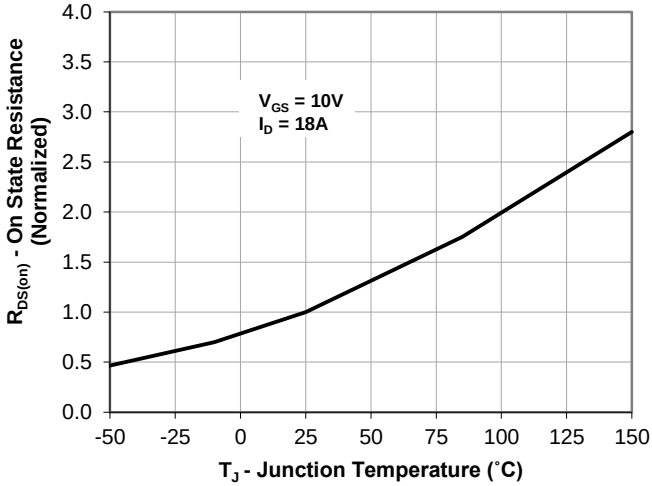
Transfer Characteristics



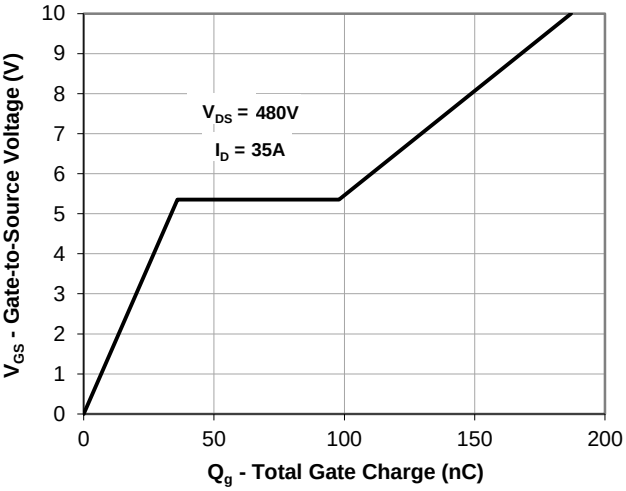
On Resistance vs Drain Current



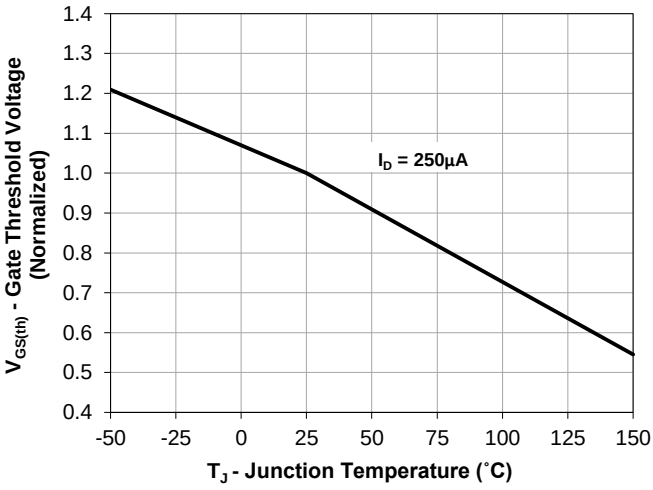
On Resistance vs Junction Temperature



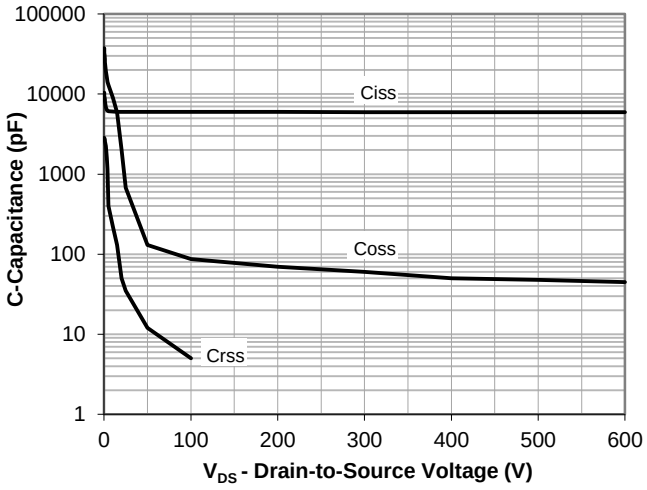
Gate Charge



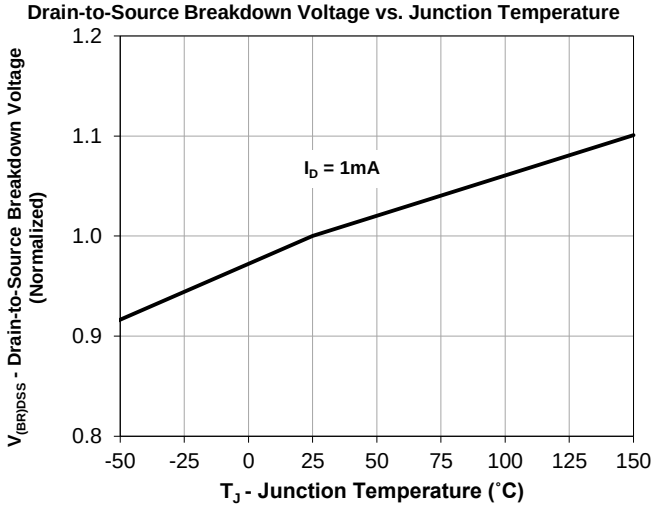
Gate Threshold Voltage vs Junction Temperature



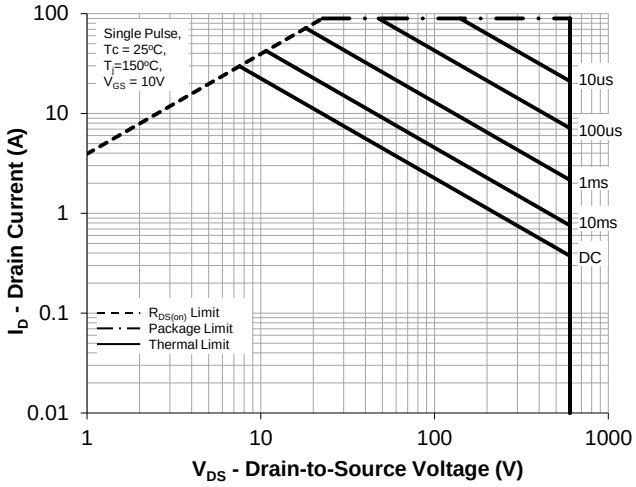
Capacitance



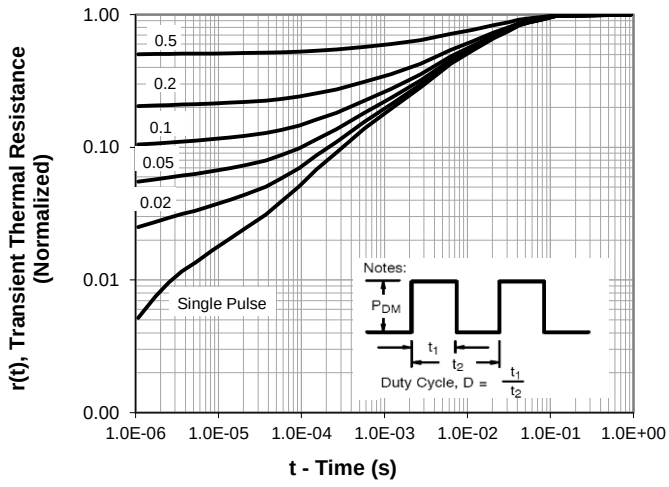
Drain-to-Source Breakdown Voltage vs. Junction Temperature

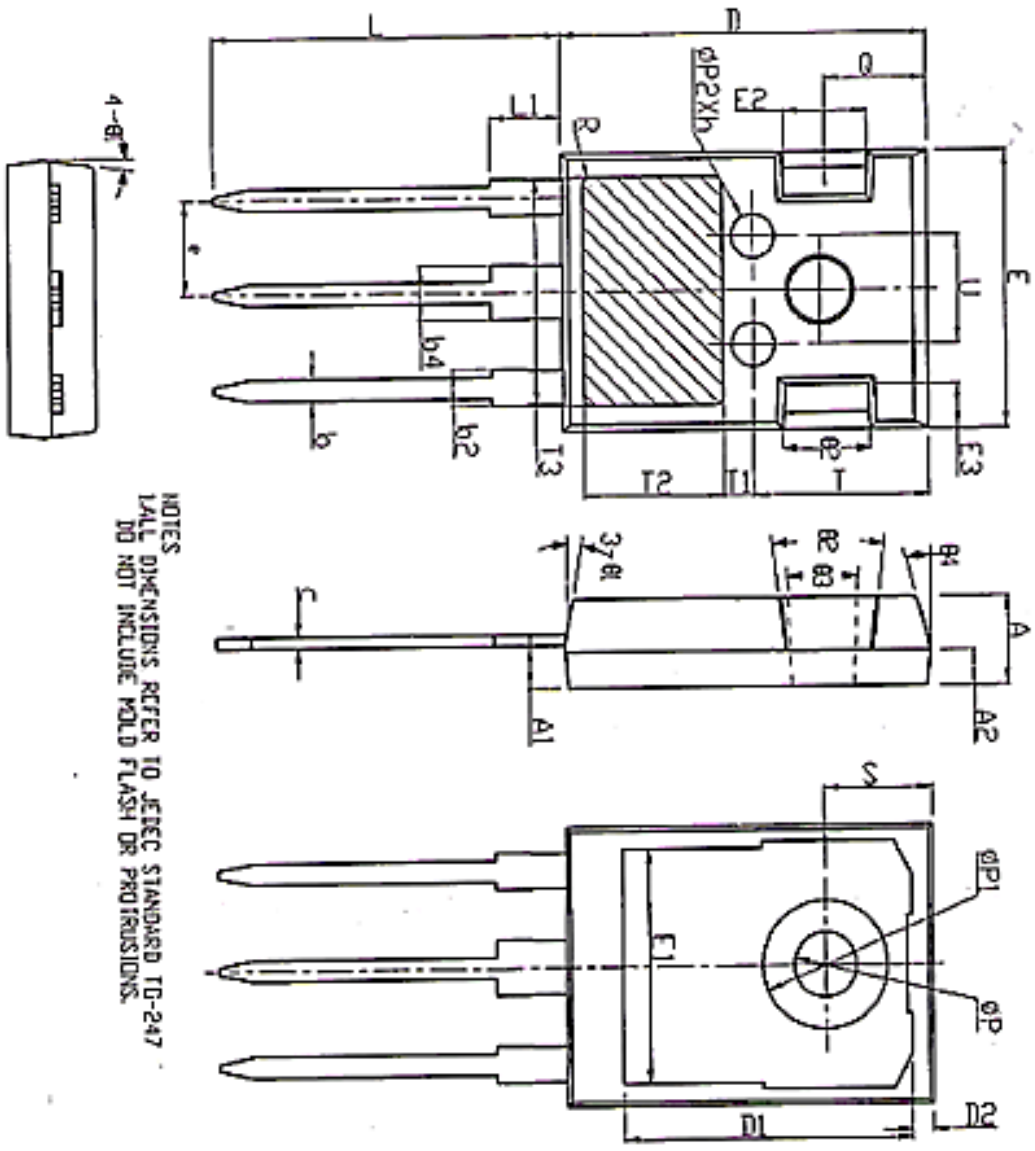


Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case





SYMBOL	COMMON DIMENSIONS MM		
	MIN	NOM	MAX
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	1.21	1.26
b2	1.96	2.01	2.06
b4	2.96	3.01	3.06
c	0.59	0.61	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e		5.44 BSC	
h	0.05	0.10	0.15
L	19.80	19.92	20.10
L1	—	—	4.30
ΦP	3.50	3.60	3.70
ΦP1	—	—	7.30
ΦP2	2.40	2.50	2.60
Q	5.60	5.80	6.00
S		6.15 BSC	
R		0.50 BSC	
T	9.80	-	10.20
T1		1.65 REF	
T2		8.00 REF	
T3		12.80 REF	
U	6.00	—	6.40
θ1	6°	7°	8°
θ2	4°	5°	6°
θ3	1°	—	1.5°
θ4	14°	15°	16°

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

Marking Information

YY = Last two digits of the year

WW = Work week calendar on Icemos subcon assembly & test house

***** = Initial for Icemos subcon assembly and test house

XXXX = Wafer Lot ID

00 = may be used for wafer ID in a special case.
= "00" is used unless specified.

ICE30N60 = ICE is Icemos logo and 30N60 is a designated device part number